FIG. 1

a ... FEEDBACK BUS
b ... OUTPUT IMAGE BUS
c ... ADDRESS BUS
d ... INPUT IMAGE BUS
e ... ADDRESS BUS
M1-M4 ... MEMORY
101 ... DATA FLOW CONTROL PART
103 ... STATUS REGISTER
105 ... FEEDBACK FRAME MEMORY

FIG. 2

a ... EXEMPLARY STATUS REGISTER
b ... STANDBY
c ... INPUT
d ... PROCESSING
e ... END OF PROCESSING
f ... OUTPUT

FIG. 3

a ... FLOW OF PROCESSING OF DATA FLOW CONTROL PART
b ... PROCESSING OF DATA FLOW CONROL PART
c ... END
S101 ... CONFIRM CONTENTS OF STATUS REGISTER
S103 ... ANY MPU IN STANDBY STATE ?
S105 ... INSTRUCT MPU
S107 ... ALL DATA COMPLETELY PROCESSED ?

FIG. 4

a ... FLOW OF PROCESSING OF MPU
b ... PROCESSING OF MPU
S201 ... STANDBY
S203 ... INSTRUCTION RECEIVED ?
S205 ... CHANGE CONTENTS OF STATUS REGISTER
STANDBY = 0 , INPUT = 1
S207 ... CAPTURE INPUT DATA

S209 ... STORE ADDRESS DATA
S211 ... CHANGE CONTENTS OF STATUS REGISTER
INPUT = 0 , PROCESSING = 1
S213 ... EXECUTE IMAGE PROCESSING
S215 ... CHANGE CONTENTS OF STATUS REGISTER
PROCESSING = 0 , END OF PROCESSING = 1
S217 ... STANDBY
S219 ... OUTPUT INSTRUCTION RECEIVED ?
S221 ... CHANGE CONTENTS OF STATUS REGISTER
END OF PROCESSING = 0 , OUTPUT = 1
S223 ... OUTPUT PROCESSED DATA AND ADDRESS DATA
S225 ... CHANGE CONTENTS OF STATUS REGISTER
OUTPUT = 0 , STANDBY = 1

FIG. 5

a ... INPUT DATA
b ... OUTPUT DATA
c ... ADDRESS DATA

FIG. 6

a ... SCANNER MPU
b ... INPUT
c ... OUTPUT
d ... SYNCHRONIZATION
e ... INPUT CLK
f ... OUTPUT CLK
203 ... PRINTER MPU
205 ... DATA FLOW CONTROL PART
207 ... STATUS REGISTER
209, 227 ... SELECTOR
211a-211d, 215a-215d ... ADDRESS FIFO
213a-213d, 217a-217d ... IMAGE DATA FIFO

FIG. 7

a ... OUTPUT IMAGE
215a-215d ... ADDRESS FIFO

217a-217d ... IMAGE DATA FIFO
229 ... MIN VALUE DETECTION CIRCUIT

FIG. 8

a ... OPERATION OF SELECTOR 227
b ... START OUTPUT
c ... END
S301 ... ACTIVATE RE OF EACH FIFO MEMORY BY ONE PIXEL
AND STORE READ DATA IN buf
S303 ... DETECT min VALUE FROM ADDRESS DATA STORED IN buf
S305 (i) ... OUTPUT IMAGE DATA CORRESPONDING TO min VALUE
(ii) ... ACTIVATE RE OF FIFO CORRESPONDING TO min VALUE
BY ONE PIXEL AND STORE READ DATA IN buf
S307 ... ALL DATA OUTPUT ?

FIG. 9

a ... INPUT
b ... OUTPUT
L1, L2 ... LINE MEMORY
301 ... INPUT BUFFER MEMORY
305 ... MEMORY CONTROLLER
307 ... COUNT REGISTER

FIG. 10

a ... MEMORY CONTROLLER
b ... REGISTER × MPU NUMBER
c ... LINE MEMORY ADDRESS
d ... INDICATES LINE MEMORY L1 OR L2

FIG. 11

a ... LOWER Nbit
b ... UPPER bit

FIG. 12

a ... PROCESSING OF CPU
b ... END

S401 ... CONFIRM FREE STATE OF MPU
S403 ... FREE MPU PRESENT ?
S405 ... INSTRUCT FREE MPU TO PERFORM PROCESSING
S407 ... WRITE LOWER N bits OF ADDRESS SUBJECTED TO PROCESSING + 1 bit IN REGISTER OF MEMORY CONTROLLER
S409 ... ALL DATA COMPLETELY PROCESSED ?

FIG. 13

a ... PROCESSING OF MPU
S501 ... STANDBY (WAIT FOR INSTRUCTION FROM CPU)
S503 ... READ DATA SUBJECTED TO PROCESSING FROM INPUT BUFFER MEMORY
S505 ... PROCESSING STATE
S507 ... PROCESSING TERMINATED ?
S509 ... OUTPUT RESULT OF PROCESSING TO MEMORY CONTROLLER

FIG. 14

a ... MEMORY CONTROLLER
S601 ... INITIALIZE COUNT REGISTER
S603 ... RECEIVE PROCESSED DATA FROM MPU
S605 ... WRITE PROCESSED DATA IN CORRESPONDING ADDRESS OF LINE MEMORY L1 OR L2 ON THE BASIS OF ADDRESS IN REGISTER
S607 ... STORE QUANTITY OF WRITING IN EACH LINE MEMORY IN COUNT REGISTER
S609 ... VALUE OF COUNT REGISTER EQUAL TO PRESCRIBED VALUE ?
S611 ... INSTRUCT TO OUTPUT DATA FOR PRESCRIBED VALUE

FIG. 15

a ... INPUT BUFFER MEMORY DATA
b ... ADDRESS DATA
c ... LINE MEMORY
d ... COUNT REGISTER

FIG. 16

a ... PRESCRIBED VALUE = n

b ... LINE MEMORY
c ... COUNT REGISTER
d ... UNPROCESSED (MPU IN PROCESSING)
e ... MPU TERMINATES PROCESSING ON n-1-TH DATA
f ... WRITE RESULT OF PROCESSING
g ... OUTPUT SIGNAL IN SYNCHRONIZATION WITH CLK
h ... INITIALIZATION

FIG. 17

401 ... INPUT BUFFER MEMORY
403 ... OUTPUT BUFFER MEMORY
405 ... ADDRESS MEMORY
407 ... MEMORY CONTROLLER
409 ... DATA FLOW CONTROL PART

FIG. 18

a ... INPUT BUFFER MEMORY
b ... OUTPUT BUFFER MEMORY
c ... ADDRESS MEMORY

FIG. 19

a ... DATA FLOW CONTROL PART
b ... DATA CONTROL
c ... END
S701 ... CONFIRM FREE STATE OF MPU
S703 ... FREE MPU PRESENT ?
S705 ... INSTRUCT FREE MPU TO PERFORM PROCESSING
S707 ... ALL DATA COMPLETELY PROCESSED ?

FIG. 20

a ... FLOW OF PROCESSING MPU
b ... PROCESSING OF MPU
S801 ... STANDBY (WAIT FOR INSTRUCTION FROM DATA FLOW CONTROL PART)
S803 ... READ DATA SUBECTED TO PROCESSING FROM INPUT BUFFER MEMORY

S805 ... PROCESSING STATE

S807 ... PROCESSING TERMINATED ?

S809 ... OUTPUT RESULT OF PROCESSING TO OUTPUT BUFFER MEMORY AND CORRESPONDING ADDRESS TO ADDRESS MEMORY

FIG. 21

a ... FLOW OF OUTPUT FROM OUTPUT BUFFER MEMORY

b ... END

S901 ... INITIALIZE COUNTER

S903 ... INITIALIZE ADDRESS T

S905 ... READ DATA ADR OF ADDRESS T FROM ADDRESS MEMORY

S907 ... ADR MATCH WITH COUNTER OUTPUT ?

S909 ... OUTPUT DATA Dout OF ADDRESS ADR OF OUTPUT BUFFER MEMORY

S911 ... INCREMENT VALUE OF COUNTER

S913 ... ALL DATA COMPLETELY PROCESSED ?

S915 ... INCREMENT ADDRESS T OF ADDRESS MEMORY

FIG. 22

a ... ADDRESS MEMORY

b ... OUTPUT BUFFER MEMORY

c ... SEARCH ADDRESS MEMORY FOR n-1

d ... OUTPUT DATA Dn-1 OF ADDRESS i+k OF n-1 FROM OUTPUT BUFFER MEMORY

e ... SEARCH ADDRESS MEMORY FOR n

f ... OUTPUT DATA Dn OF ADDRESS i OF n FROM OUTPUT BUFFER MEMORY

g ... OUTPUT DATA

FIG. 23

a ... INPUT IMAGE

b ... OUTPUT IMAGE

903 ... A-D CONVERSION

905 ... SHADING CORRECTION AND LOG CONVERSION

907 ... VARIABLE POWER

909 ... MTF CORRECTION
911 ... γ CORRECTION
913 ... BINARIZATION
915 ... INPUT MEMORY
919 ... OUTPUT MEMORY

FIG. 24

a ... FEEDBACK BUS
b ... OUTPUT IMAGE BUS
c ... INPUT IMAGE BUS
951 ... FEEDBACK FRAME MEMORY
952 ... DATA FLOW CONTROL PART
953 ... STATUS REGISTER

FIG. 26

a ... INPUT DATA
b ... OUTPUT DATA

[Document Name] Abstract

[Abstract]

[Subject] To efficiently process image data in a circuit dividing single image data into a plurality of data and processing the data with a plurality of MPUs in parallel with each other.

[Solving Means] MPU1 to MPU4 process image data input through an input image data in parallel with each other. An address bus inputs addresses of the image data, and address memories M1 to M4 provided on the MPU1 to MPU4 store the addresses of the image data processed by the MPUs respectively. When the image data are completely processed, the image data are output through an output image bus while the addresses of the image data are output through the address bus.

[Selected Drawing] Fig. 1